CLAIMS

What is claimed is:

1. A protection circuit, comprising:

a transistor power estimation circuit;

a power estimate filtering circuit connected to the transistor power estimating circuit;

a transistor control circuit connected to the power estimate filtering circuit;

a transistor temperature adjustment circuit connected to the transistor power estimating circuit; and

a transistor maximum current limiting circuit connected to the transistor power estimating circuit.

2. The circuit of claim 1, wherein the transistor power estimation circuit includes:

a transistor current sensing circuit;

a transistor voltage sensing circuit; and

a summing circuit connected to the transistor current and voltage sensing circuits.

3. The circuit of claim 1, wherein the transistor power estimation circuit is a single slope power estimation circuit.

4. The circuit of claim 1, wherein the transistor power estimation circuit is a two-slope power estimation circuit.

5. The circuit of claim 1, wherein the transistor power estimation circuit is a four-slope power estimation circuit.

6. The circuit of claim 1, wherein the transistor power estimation circuit is a multi-slope power estimation circuit.

7. The circuit of claim 1, wherein the power estimate filtering circuit includes an averaging circuit.

8. The circuit of claim 1, wherein the power estimate filtering circuit includes a transistor thermal equivalent circuit.

9. The circuit of claim 1, wherein the power estimate filtering circuit includes a resister capacitor network.

10. The circuit of claim 1, wherein the transistor maximum current limiting circuit includes a predetermined number of diodes and a resistor.

11. The circuit of claim 1, wherein the transistor control circuit includes a transistor.

12. The circuit of claim 1, wherein the transistor temperature adjustment circuit includes a thermistor.

13. The circuit of claim 1, wherein the transistor temperature adjustment circuit is integrated into the transistor power estimation circuit.

14. The circuit of claim 1, wherein the transistor control circuit includes an optocoupler.

15. A protection method, comprising the steps of:

generating a power estimate of power dissipated by a power

transistor;

filtering the power estimate to eliminate any transient power estimates and to generate a filtered power estimate; and

comparing the filtered power estimate to a predetermined power limit and, when the filtered power estimate exceeds the predetermined power limit, generating a power transistor control signal that causes the power transistor to reduce its power dissipation.

16. The method of claim 15, further comprising the steps of adjusting the filtered power estimate so that it varies as a function of power transistor operating temperature.

17. The method of claim 15, further comprising the steps of limiting current output by the power transistor to a predetermined maximum level.

18. The method of claim 15, wherein the power transistor control signal causes the power transistor to reduce its power dissipation by reducing power supply voltage applied to the power transistor.

19. The method of claim 15, wherein the power transistor control signal causes the power transistor to reduce its power dissipation by reducing base current flowing into the power transistor.

20. The method of claim 15, wherein the power transistor control signal causes the power transistor to reduce its power dissipation by reducing power supply voltage applied to the power transistor and reducing base current flowing into the power transistor.

21. A method of estimating junction temperature of a transistor, comprising the steps of:

generating a piecewise linear approximation of the transistor's power dissipation;

varying the piecewise linear approximation as a function of transistor temperature; and

averaging the temperature varying, piecewise linear approximation to generate an estimate of transistor junction temperature.